

Date Code: AP.PRE.REQ

PTO/SB/33 (07/05)

Approved for use through xx/xx/200x. OMB 0651-00xx  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE  
The Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional) <b>ITL.1047US (P17449)</b>
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR		Application Number <b>10/726,418</b>
on <b>July 19, 2006</b>		Filed <b>December 3, 2003</b>
Signature 		First Named Inventor <b>John I. Garney</b>
Typed or printed name <b>Nancy Meshkoff</b>		Art Unit <b>2186</b>
		Examiner <b>Paul W. Schlie</b>
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.		
This request is being filed with a notice of appeal.		
The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.		
<p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <b>28,994</b></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p>		
 <b>Timothy N. Trop</b> Typed or printed name <b>(713) 468-8880</b> Telephone number <b>July 19, 2006</b> Date		
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.		
<input type="checkbox"/> *Total of _____ forms are submitted.		

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney or Applicant:

John I. Garney

§ Art Unit: 2186

Serial No.: 10/726,418

§ Examiner: Paul W. Schlie

Filed: December 3, 2003

§ Docket: ITL.1047US  
P17449

For: Write-Back Disk Cache

§ Assignee: Intel Corporation

§

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**STATEMENT IN SUPPORT OF PRE-APPEAL REQUEST FOR REVIEW**

Sir:

Pre-Appeal Review is requested because the rejection is based on the application itself. In other words, the pending application is the only art cited to teach the claimed invention.

In the background, at page 2, lines 18-23, it is noted that during system startup, a disk may be accessed by a basic input/output system disk request. Later in startup, after an operating system loads the disk drive, the software driver, the disk may be accessed by the operating system.

Just because it is possible to access the disk before system startup does not mean that it is anticipated or obvious to write a dirty cache line to a disk prior to disk driver loading and to monitor the disk write request prior to disk driver loading.

In other words, there is nothing within the present application that teaches writing a dirty cache line to a disk drive prior to disk loading. The mere fact that you can write something to the disk drive prior to disk driver loading is not sufficient to meet the claimed invention. Nobody ever monitored for a disk write request prior to disk driver loading and no

Date of Deposit: July 19, 2006

I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

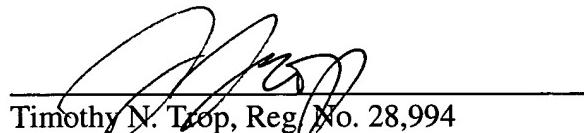
Nancy Meshkoff

reference is cited to teach the same. Therefore neither element is taught within the background of the present application and there is no basis for the rejection.

Likewise the requirement that the stack be illustrated is noted. It is apparently premised on the fact that dependent claim 7 refers to a stack. But a stack is not a physical object. It is merely an organization in software. For example, "stack" is defined as "hardware registers or a reserved amount of memory used for arithmetic calculations or to keep track of internal operations". *See* McGraw-Hill Computer Desktop Encyclopedia (attached). Thus there does not appear to be any way to illustrate a stack other than to simply draw a box. It is unclear where the box would be drawn or how drawing such a box would in any way help the present application. Given this quandary, it seems that there is no reason to draw software stacks since processor stacks are well-known, and it is known how they operate and where they reside.

Therefore reconsideration is requested.

Respectfully submitted,



\_\_\_\_\_  
Timothy N. Trop, Reg. No. 28,994  
TROP, PRUNER & HU, P.C.  
1616 S. Voss Road, Suite 750  
Houston, TX 77057  
713/468-8880 [Phone]  
713/468-8883 [Fax]

Attorneys for Intel Corporation

# BEST AVAILABLE COPY

stack overflow 925

**SSE** (1) (Single SIMD Extensions) A group of 70 instructions added to the Pentium III chip that improves 3-D graphics performance. It includes floating point capability for 3-D geometry calculations. SSE is the second set of enhancements to the Intel CPU chips for multimedia operations (MMX was the first). The Pentium 4 added 144 more instructions known as SSE2. SSE was originally code named the Katmai New Instructions (KNI), because the Pentium III was code named Katmai. See *Pentium III, MMX* and *SIMD*.

(2) A Protected Mode full-screen editor in OS/2.

**SSI** (1) See *server-side include* and *single-system image*.

(2) (Small-Scale Integration) Less than 100 transistors on a chip. See *MSI, LSI, VLSI* and *ULSI*.

**SSJS** (Server-Side JavaScript) A JavaScript interpreter for running JavaScript programs on the server. It includes a library of objects and functions for accessing databases, sending e-mail and performing other tasks. Contrast with *CSJS*.

**SSL** (Secure Sockets Layer) The leading security protocol on the Internet. When an SSL session is started, the server sends its public key to the browser, which the browser uses to send a randomly-generated secret key back to the server in order to have a secret key exchange for that session. Developed by Netscape, SSL has been merged with other protocols and authentication methods by the IETF into a new protocol known as Transport Layer Security (TLS). See *TLS, security protocol* and *public key cryptography*.

**SSP** (1) (Service Switching Point) The local exchange node in an SS7 telephone network. The SSP can be part of the voice switch or in a separate computer connected to it. The SSP creates SS7 signaling messages that are sent to a "service control point" (SCP) to query databases for subscriber service and routing information. See *A/N* and *SCP*.

(2) (Storage Service Provider) A third party that manages the storage facilities for an enterprise. The storage devices can be on the customer's premises or at the SSP's site connected to the customer's machines via fiber-optic links. See *ASP*.

(3) (Switch to Switch Protocol) The protocol used in DLSw that locates resources and routes messages.

(4) (System Support Program) A multiuser, multitasking operating system from IBM that is the primary control program for the System/34 and System/36.

**stack** (1) A set of hardware registers or a reserved amount of memory used for arithmetic calculations or to keep track of internal operations. Stacks keep track of the sequence of routines called in a program. For example, one routine calls another, which calls another and so on. As each routine is completed, the computer returns control to the calling routine all the way back to the first one that started the sequence. Stacks used in this way are LIFO based: the last item, or address, placed (pushed) onto the stack is the first item removed (popped) from the stack.

Stacks are also used to hold interrupts until they can be serviced. Used in this manner, they are FIFO stacks, in which the first item onto the stack is the first one out of the stack. See *DOS Stacks*.

An "internal stack failure" is a fatal error which means that the operating system has lost track of its next operation. Restarting the computer usually corrects this, otherwise the operating system may have to be re-installed. See *stack dump* and *stack fault*.

(2) See *protocol stack* and *HyperCard*.

**stackable hub** A type of Ethernet hub that can be expanded by daisy chaining additional hubs together via dedicated ports for that purpose. They are designed to stack vertically and be treated as a single domain by the network management software.

**stack dump** The contents of a stack. A stack dump is often displayed when an error occurs. See *stack*.

**stacker** (1) An output bin in a document feeding or punched card machine. Contrast with *hopper*.

(2) (Stacker) A realtime compression program from Stac Electronics, Carlsbad, CA ([www.stac.com](http://www.stac.com)) that doubles the disk capacity of a DOS, Windows, Mac or OS/2 computer.

**stack fault** An error condition that occurs when the stack is either empty or full. See *stack overflow*.

**stack overflow** An error condition that occurs when there is no room in the stack for a new item. This error condition can also occur when other things go awry; for example, a bad expansion board or one that isn't seated properly in the slot can cause erratic signals eventually leading to a stack overflow error message. Contrast with *stack underflow*. See *stack*.